Shift Registers and Multiplexers
Shift Registers

- Used to temporarily hold, copy, and bit-shift data words during transmission of data
- Constructed from a row of connected flip-flops
- Can handle parallel movement of data bits as well as serial movement and also can be used to convert from parallel to serial or from serial to parallel
Parallel-In/Serial Out Shift Register

The diagram shows a 74HC165 parallel-in/serial-out shift register. The key features include:

- **Digital Inputs**: D0, D1, D2, D3, D4, D5, D6, D7
- **Clock (CLK)**
- **Control Inputs**: PL, SDI, CKE
- **Outputs**: Q7

The register has parallel inputs for data entry and a serial output for data retrieval. The truth table and timing characteristics are also indicated in the diagram.
Parallel-In/Serial Out Shift Register

Set PD2/PD3 as output pins
Set PD4 as input pins
Set PD2/PD3 high

1. Set PD3 LOW
2. Set PD3 HIGH (This saves the current state of the inputs in the PI/SO-S chip)
3. Set PD2 LOW
4. Set PD2 HIGH (First clock signal)
5. Read PD4 to get saved Input H
6. Set PD2 LOW
7. Set PD2 HIGH (Second clock signal)
8. Read PD4 to get saved Input G
9. Set PD2 LOW
10. Set PD2 HIGH (Third clock signal)
11. Read PD4 to get saved Input F
12. …. Repeat clock signal on PD2 and read on PD4 to get rest of saved inputs….
Parallel-In/Serial Out Shift Register

Digital Inputs

74HC165 -1

Digital Inputs

74HC165 -2
Parallel-In/Serial Out Shift Register

1. Set PD2 and PD3 as output pins
2. Set PD4 and PD5 as input pins
3. Set PD2 and PD3 High

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1. Set PD3 LOW
2. Set PD3 HIGH (This saves the current state of the inputs in the PI/SO-S chip)
3. Set PD2 LOW
4. Set PD2 HIGH (First clock signal)
5. Read PD4 to get saved Input H1
6. Read PD5 to get saved Input H2
7. Set PD2 LOW
8. Set PD2 HIGH (Second clock signal)
9. Read PD4 to get saved Input G1
10. Read PD5 to get saved Input G2
11. Set PD2 LOW
12. Set PD2 HIGH (Third clock signal)
13. Read PD4 to get saved Input F1
14. Read PD5 to get saved Input F2
15. …. Repeat clock signal on PD2 and read on PD4, PD5 to get rest of saved inputs…. 
Serial-In/Parallel-Out Shift Register

HC11 PD3
HC11 PD2
74LS164

Digital Outputs
Serial-In/Parallel-Out Shift Register

1. Set PD2 and PD3 and PD4 as output pins
2. Set PD3 LOW
3. Set PD3 HIGH

1. Set PD3 LOW
2. Set PD3 HIGH (This resets the PO/SI-S chip and sets Output QA-H LOW)
3. Set PD4 to desired state (LOW/HIGH) of Output QH
4. Set PD2 LOW
5. Set PD2 HIGH (First clock signal. Desired state of Output QH is shifted into Output QA pin)
6. Set PD4 to desired state (LOW/HIGH) of Output QG
7. Set PD2 LOW
8. Set PD2 HIGH (Second clock signal. Desired state of Output QG is shifted into Output QA pin. Desired state of Output QH is shifted into Output QB pin.)
9. Set PD4 to desired state (LOW/HIGH) of Output QF
10. Set PD2 LOW
11. Set PD2 HIGH (Third clock signal. Desired state of Output QF is shifted into Output QA pin. Desired state of Output QG is shifted into Output QB pin. Desired state of Output QH is shifted into Output QC pin.)
12. …. Repeat clock signal on PD2 and set on PD4 as needed to set the remaining output pins.

When all 8 desired states of Output QA-H are clocked in, the desired states of Output QA-H will line up with appropriate Output QA-H pins.
Serial-In/Parallel-Out Shift Register

[Diagram of a Serial-In/Parallel-Out Shift Register with labels for HC11 PD4, HC11 PD3, and HC11 PD2.]
Serial-In/Parallel-Out Shift Register

1. Set PD2 and PD3 and PD4 as output pins
2. Set PD3 LOW
3. Set PD3 HIGH

1. Set PD3 LOW
2. Set PD3 HIGH (This resets the PO/SI-S chip and sets Output QA-P LOW)
3. Set PD4 to desired state (LOW/HIGH) of Output QP
4. Set PD2 LOW
5. Set PD2 HIGH (First clock signal. Desired state of Output QP is shifted into Output QA pin)
6. Set PD4 to desired state (LOW/HIGH) of Output QO
7. Set PD2 LOW
8. Set PD2 HIGH (Second clock signal. Desired state of Output QO is shifted into Output QA pin. Desired state of Output QP is shifted into Output QB pin.)
9. Set PD4 to desired state (LOW/HIGH) of Output QN
10. Set PD2 LOW
11. Set PD2 HIGH (Third clock signal. Desired state of Output QN is shifted into Output QA pin. Desired state of Output QO is shifted into Output QB pin. Desired state of Output QP is shifted into Output QC pin.)
12. …. Repeat clock signal on PD2 and set on PD4 as needed to set the remaining output pins. When all 16 desired states of Output QA-P are clocked in, the desired states of Output QA-P will line up with appropriate Output QA-P pins.
Multiplexer/De-multiplexer

- **74LS151 8 line to 1 line multiplexer**
Multiplexer/De-multiplexer

- 74LS138 De-multiplexer